WHAT IS CLAIMED IS:

1. An integrated circuit memory device, comprising:

a delay locked loop (DLL) circuit;

a DLL power supply supplying power to the DLL circuit; and

a control signal generator controlling the DLL power supply to selectively supply power to the DLL circuit during a refresh mode of the integrated circuit memory device based on a selection signal.

2. The device of claim 1, wherein first clock signal based on a reference clock signal and locking information, the locking information being information on a phase relationship between the first clock signal and the reference clock signal; and

the control signal generator further controlling the DLL circuit to selectively reset the locking information during the refresh mode of the integrated circuit memory device based on the selection signal.

3. The device of claim 2, wherein the first clock signal is one of a feedback clock signal, feedback within the DLL circuit, and an internal clock signal generated by the DLL circuit.

4. The device of claim 2, wherein the DLL circuit comprises:

a phase detector detecting a phase difference between the first clock

signal and the reference clock signal;

a variable delay circuit adjusting the locking information based on the phase difference, and delaying the reference clock signal to produce the first clock signal based on the locking information; and

a disabling circuit disabling the adjusting function of the variable delay circuit during the refresh mode.

5. The device of claim 4, wherein the disabling circuit causes the reference clock signal to maintain a steady logic state during the refresh mode.

6. The device of claim 1, further comprising:

a selection signal generator generating the selection signal based on a mode register set command received by the integrated circuit memory device.

7. The device of claim 1, wherein the selection signal is an externally supplied signal.

8. The device of claim 1, further comprising:

a fuse circuit to generate the selection signal during the refresh mode.

9. The device of claim 1, further comprising:

a first command decoder decoding a refresh command to generate a refresh mode indication signal indicating whether the integrated circuit

memory device is in the refresh mode, and sending the refresh mode indication signal to the control signal generator and the DLL circuit.

10. The device of claim 9, further comprising:

a second command decoder decoding a DLL command to generate a DLL indication signal indicating whether the DLL power supply is to supply power to the DLL circuit during the refresh mode, and sending the DLL indication signal to the control signal generator as the selection signal.

11. The device of claim 1, wherein the control signal generator initially controls the DLL power supply to supply power to the DLL circuit and then controls the DLL power supply to cut power to the DLL circuit.

12. The device of claim 1, wherein

the DLL circuit generates a first clock signal based on a reference clock signal and locking information, the locking information being information on a phase relationship between the first clock signal and the reference clock signal;

the control signal generator controls the DLL circuit to selectively reset the locking information during the refresh mode of the integrated circuit memory device based on the selection signal; and

the control signal generator initially controls the DLL circuit to maintain the locking information and then controls the DLL circuit to reset

the locking information.

13. The device of claim 1, further comprising:

a row address decoder generating word line signals in sequence during the refresh mode based on an oscillating signal; and

an oscillator generating the oscillating signal during the refresh mode.

14. The device of claim 13, wherein the oscillator generates the selection signal such that the control signal generator controls the DLL power supply to cut power to the DLL circuit at least one period of time after generating the oscillating signal.

15. The device of claim 14, wherein the period of time is a period of time for the row address decoder to generate each word line signal several times.

16. The device of claim 14, wherein the period of time is a period of time for the row address decoder to generate each word line signal once.

17. The device of claim 14, wherein

the DLL circuit generates a first clock signal based on a reference clock signal and locking information, the locking information being information on a phase relationship between the first clock signal and the reference clock signal; and

the control signal generator controls the DLL circuit to selectively reset the locking information during the refresh mode of the integrated circuit memory device based on the selection signal; and

the oscillator generates the selection signal such that the DLL circuit is turned off a period of time after generating the oscillating signal.

18. The device of claim 1, wherein

the DLL circuit is reset based on a reset signal; and

the control signal generator selectively generates the reset signal during the refresh mode of the integrated circuit memory device.

19. A method of controlling a delay lock loop (DLL) circuit of an integrated circuit memory device, comprising:

controlling a DLL power supply to selectively supply power to the DLL circuit during a refresh mode of the integrated circuit memory device.

20. An integrated circuit memory device, comprising:

a delay locked loop (DLL) circuit receives an external clock signal and generates an internal clock signal;

wherein the DLL circuit is turned on during a first refresh operation and is turned off during a second refresh operation.

21. The device of claim 20, further comprising a selection signal generator for

selecting a refresh operation between the first refresh operation and the second refresh operation.

22. The device of claim 21, wherein the selection signal generator generating a selecting signal.

23. The device of claim 22, wherein the selection signal is generated by programming means

24. The device of claim 23, wherein the programming means is a mode register set command.

25. The device of claim 22, wherein the selection signal is input from an external pin.

26. The device of claim 22, wherein the selection signal is a fuse information signal.

27. An integrated circuit memory device, comprising:

a delay locked loop (DLL) circuit,the DLL circuit generates a first clock signal based on a reference clock signal and locking information, the locking information being information on a phase relationship between the first clock signal and the reference clock signal; and

a control signal generator controlling the DLL circuit to selectively reset the locking information during a refresh mode of the integrated circuit memory device based on a selection signal.

28. The device of claim 27, wherein the control signal generator further controls the DLL circuit to cease updating the locking information and enter a power-off state.